FACULTY OF SCIENCE

B.Sc. III year (V - Semester) (PRACTICAL) Examination

(With effect from Annual 2018)

Subject: Electronics (New Syllabus)

Paper-V: Digital Electronics

QUESTION BANK

Time: 2 Hours Max. Marks: 25

Note: Candidate may be asked to strike off any one question [among the allotted 8(eight) experiments for the batch], which he doesn't wish to attempt.

ANY ONE MAY BE ALLOTTED TO THE CANDIDATE FROM THE REST.

1. Verify the truth tables of OR, AND, NOT, NAND, NOR,X-OR logic gates of TTL 7400 series IC's.
2. Construct and verify the truth tables of OR, AND, NOT, NAND, NOR,X-OR logic gates Using discrete components.
3. Construct and verify the truth tables of Basic logic gates using NAND and NOR logic Gates (Universal Building Blocks).
4. Construct and verify De – Morgans Laws.
5. Construct and verify the truth tables of RS, D and JK Flip Flops using IC's.
6. Construct and verify the circuit table (Truth Table) of Decade counters using 7490 IC. Verify the action of stepper motor interface using a JK Flip Flop.
7. Construct a Half Adder and Full Adder circuits and verify their truth tables.
8. Using appropriate electronic simulation circuit construct a 4 bit parallel adder and Study its working.
9. Simulate a Decade counter using JK Flip Flops and verify its performance.
10. Simulate 4 – Bit Synchronous up counter using Master Slave JK Flip Flops and verify its Performance.
11. Simulate 4 – Bit Asynchronous up counter using Master Slave JK Flip Flops and verify its Performance.
12. Simulate 4:1 Multiplexer using logic gates and verify the Truth table.
13. Simulate 1:4 De - Multiplexer using logic gates and verify the Truth table.
14. Simulate Master slave JK Flip Flops using NAND gates and verify its truth table.
15. Simulate Binary to Nibble decoder (2 to 4 line) using logic gates and verify

FACULTY OF SCIENCE

B.Sc. III year (V - Semester) (PRACTICAL) Examination

(With effect from Annual 2018)

Subject: Electronics (New Syllabus)

Paper-VI: Microprocessor (8085) and Application

QUESTION BANK

Time: 2 Hours Max. Marks: 25

Note: Candidate may be asked to strike off any one question [among the allotted 8(eight) experiments for the batch], which he doesn't wish to attempt.

ANY ONE MAY BE ALLOTTED TO THE CANDIDATE FROMN THE REST

1. Write an ALP and Flow chart to perform 8 bit decimal addition of two numbers stored in consecutive memory locations.

2. Write an ALP and flow chart that performs 16 bit addition of the 16 bit numbers stored in register pairs DE and HL.

3. Write an ALP and flow chart to multiply two numbers 08_H and 05_H.

4. Write an ALP to divide 14_H by 05_H.

5. Write an ALP that picks up smallest of 5 numbers stored in consecutive memory locations and stores the result in the next memory location.

6. Write an ALP that picks up largest of 10 numbers stored in consecutive memory locations.

7. Write an ALP that arranges the given set of 10 numbers stored in consecutive memory locations in ascending order.

8. Write an ALP that arranges the given set of 10 numbers stored in consecutive memory locations in descending order.

9. Write an ALP and flow chart to subtract two numbers stored in consecutive memory locations and store the result in next memory location.

10. write an ALP and flow chart to generate a time delay of 10msec. Show the delay calculations.

11. construct an R-2R ladder network 4 bit D/A converter and verify it's working.

12. Write an ALP to rotate a stepper motor both clockwise and anticlockwise through a known angle.

13. Interface a seven segment display to a µp to study its performance.

14. Construct an A/D converter by interfacing it to the µp for temperature measurement.